2102440 Introduction to Microprocessors

Chapter 11

Interrupt Controller

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Topics

- Interrupt vector table
- Interrupt service routine
- Categories of interrupts
  - Hardware interrupts
  - Software interrupts
- 8259 Interfacing
- 8259 programming

8088/8086 Interrupts

- An interrupt is an external event which informs the CPU that a device needs its service.
- There are 256 interrupts (types): INT 00, INT 01, …, INT FF in the 8088/8086.
- When executes an interrupt, microprocessor automatically saves the flag register, the instruction pointer, and the code segment register on the stack, and goes to a fixed memory location.

Interrupt Vector Table

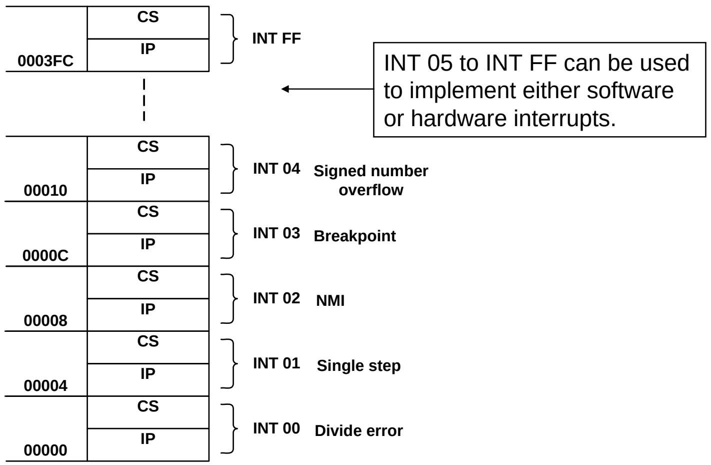
INT number	Physical address	Logical address
INT 00	00000	0000:0000
INT 01	00004	0000:0004
INT 02	00008	0000:0008
INT 03	0000C	0000:000C
INT 04	00010	0000:0010
INT 05	00014	0000:0014
…	…	…
INT FF	003FC	0000:03FC

- Interrupt goes to the memory location that is four times the value of the interrupt number.
- For example, INT 03 will go to address = 4x3 = 12 = 0000CH

Interrupt Service Routine (ISR)

- There is a program associated with every interrupt.
- When an interrupt is invoked, a CPU runs a program for a service → an interrupt service routine (ISR).
- The address of the interrupt service routine is shown in the interrupt vector table.
- Four bytes of memory are allocated for every interrupt.
- The memory space of 1024 bytes (256x4=1024) are set aside for the interrupt vector table.

Intel's List of Designated Interrupts for the 8088/8086



INT 05 to INT FF can be used to implement either software or hardware interrupts.

CALL vs INT

CALL FAR	INT nn
Jump to any location within the 1 MByte address range.	Go to a fixed memory location in the interrupt vector table.
Locate in the sequence of instructions in the program.	Externally activated hardware interrupt can come at any time.
Cannot be masked (disabled).	Can be masked.
Save CS:IP of the next instruction on the stack.	Save CS:IP of the next instruction and flag register on the stack.
Use RETF in the last instruction of its routine. ➢RETF pops CS, IP off the stack.	Use IRET in the last instruction of its routine. ➢IRET pops CS, IP, and the flag register.

Hardware Interrupts

- Three pins, in the 80x86, are associated with hardware interrupts:
  - INTR (interrupt request):
    - an input signal into the CPU which can be masked (ignored) and unmasked through CLI (disabled) and STI (enabled).
    - No specific location in the vector table assigned for INTR.
    - It uses any "INT nn: space that has not been assigned.
    - 8259 chip connects to INTR to expand # of hardware interrupts up to 64.
  - NMI (nonmaskable interrupt): INT 02
    - an input signal into the CPU that cannot be masked and unmasked using software instructions.
    - CPU will go to memory location 0008 to get the address (CS:IP) of the interrupt service routine associated with NMI.
  - INTA (interrupt acknowledge)
    - An output of the microprocessor to signal the external circuitry that the interrupt request has been acknowledged and to prepare to put its interrupt type number on the data bus.

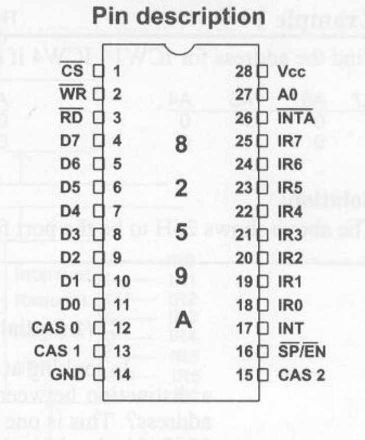
Software Interrupts

- INT nn is invoked software (sequence of code)
- Examples
  - DOS INT 21H, BIOS INT 10H.
  - INT 00 (divide error)
  - INT 01 (single step)
  - INT 03 (breakpoint)
  - INT 04 (signed number overflow)

Processing Interrupts

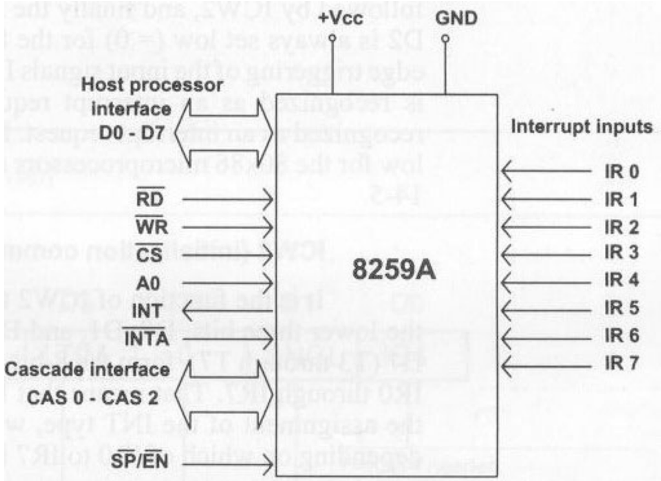
1. The flag register (2-byte register) is pushed onto the stack and SP is decremented by two.
2. IF (interrupt enable flag) and TF (trap flag) are cleared→ mask (ignore) other interrupt requests from the INTR and disable single-step.
3. The current CS:IP are pushed onto the stack → SP is decremented by 4.
4. The INT number is multiplied by 4 to get the physical address of the location of CS:IP of the interrupt service routine.
5. CPU starts to fetch and execute of the interrupt service routine from the new CS:IP.
6. CPU executes the last instruction (IRET) and get IP, CS, and flag register back from the stack.
7. CPU continues executing the code where it left off.

8259 Programmable Interrupt Controller

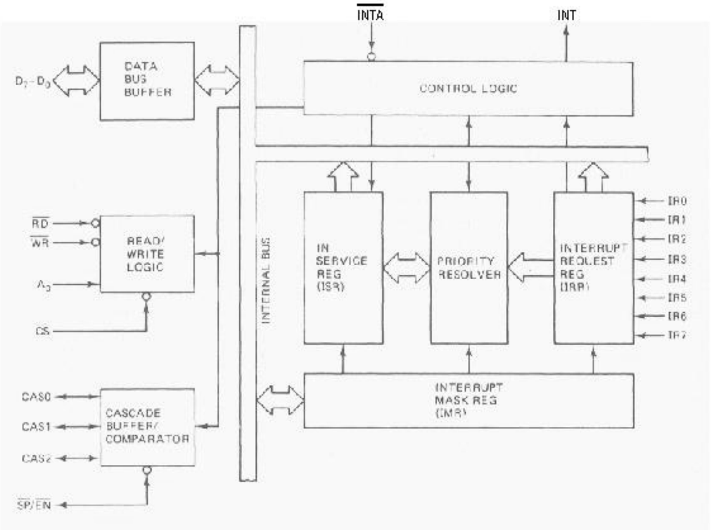


80x86 can use INTR and INTA pins to expand the number of interrupts.

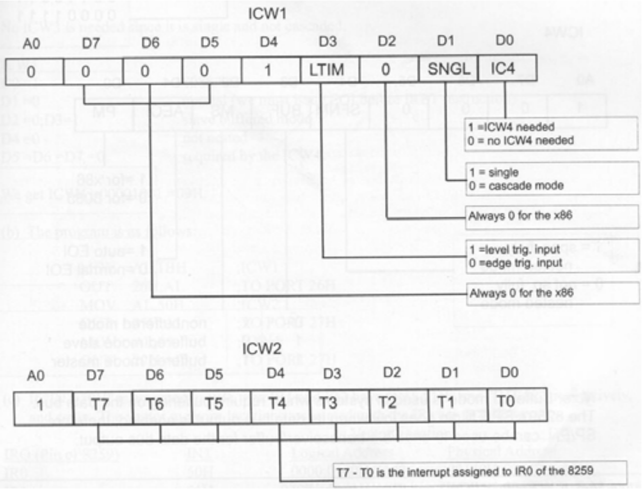
Block Diagram of the 8259A



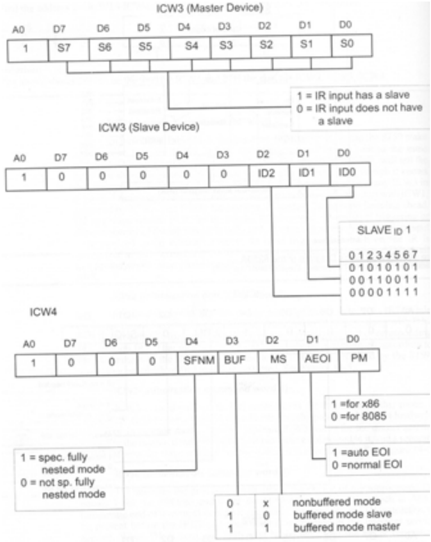
Internal Architecture of the 8259A



Initialization Command Word (ICW1, 2)

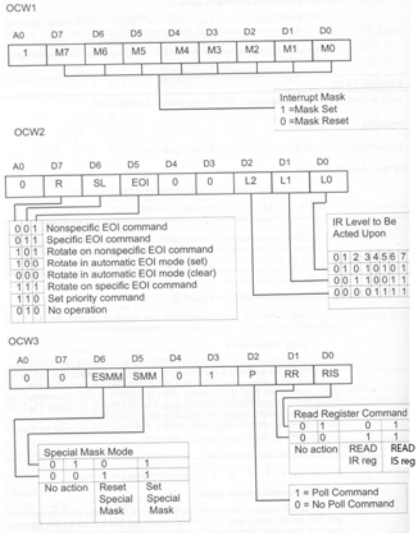


ICW 3, ICW4

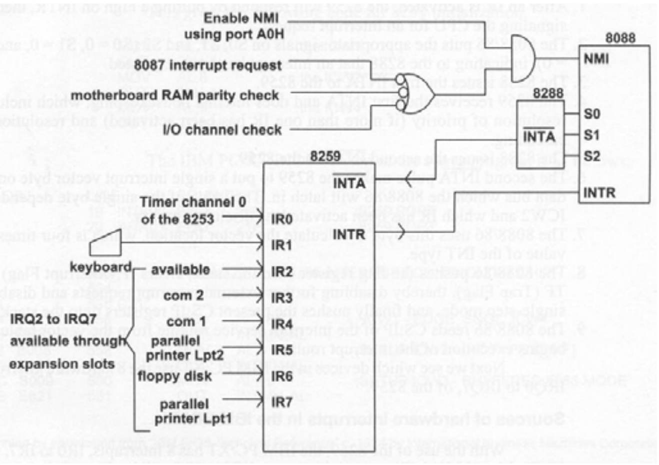


Note: Buffered mode is used in systems which require buffering on the data bus. The 8259's $\overline{SP}/\overline{EN}$ pin goes low when its data bus output is enabled; therefore, $\overline{SP}/\overline{EN}$ can be used to enable a transceiver/buffer for the data bus output.

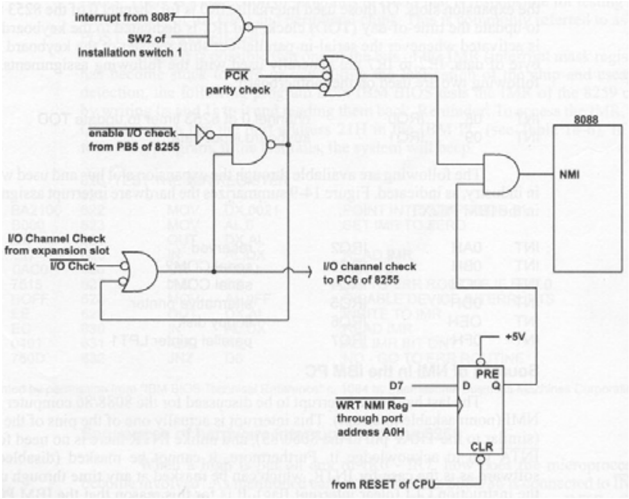
Operation Command Word (OCW)



Source of Hardware Interrupts



Sources of NMI


interrupt from 8087
SW2 of installation switch 1
$\overline{\text{PCK}}$ parity check
$\overline{\text{enable I/O check}}$ from PB5 of 8255
I/O Channel Check from expansion slot
$\overline{\text{I/O Chck}}$
I/O channel check to PC6 of 8255
8088
NMI
+5V
PRE
D
Q
D7
$\overline{\text{WRT NMI Reg}}$ through port address A0H
CLR
from RESET of CPU