2102440 Introduction to Microprocessors

Chapter 6

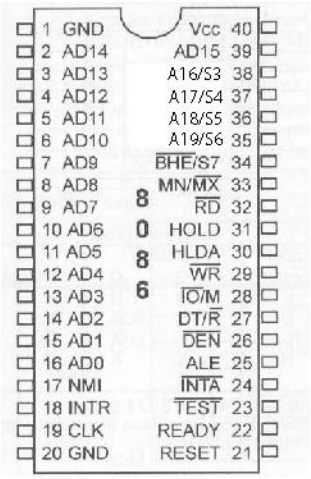
The 8086 Hardware Architecture

Suree Pumrin, Ph.D.

Topics

- Minimum-mode and maximum-mode systems
- DEMUX address/Data bus
- Bus cycle and time states

The 8086 Microprocessor



The 8086 in Minimum Mode

- It is a 40-pin dual in-line package.
- Many pins have multiple functions.
- It can work in two modes: minimum mode and maximum mode.
- Maximum mode is used when it needs to connect to an 8087 math coprocessor.
- The minimum mode is selected by making the MN/MX equal to 1.
- The maximum mode is selected by making the MN/MX equal to 0.
- Minimum mode 8086 system has one microprocessor.
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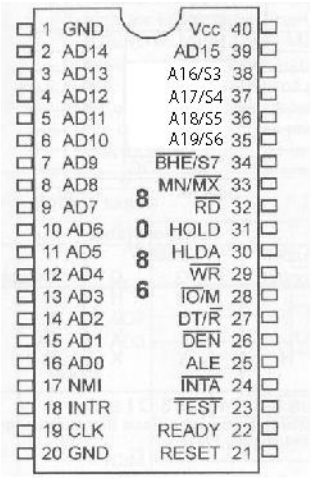
Common Signals in both Minimum and Maximum Modes

Name	Function	Type
AD15-AD0	Address/data bus	Bidirectional, 3-state
A19/S6-A16/S3	Address/status	Output, 3-state
$\overline{BHE}$ / S7	Bus High Enable/Status	Output, 3-state
$MN / \overline{MX}$	Minimum/maximum Mode control	Input
$\overline{RD}$	Read control	Output, 3-state
$\overline{TEST}$	Wait on test control	Input
READY	Wait state control	Input
RESET	System reset	Input
NMI	Nonmaskable Interrupt request	Input
INTR	Interrupt request	Input
CLK	System clock	Input
V_{CC}	+5 V	Input
GND	Ground	Input

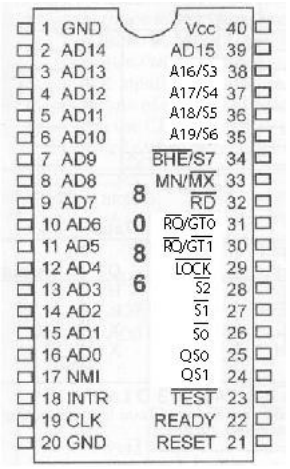
Unique Minimum Mode Signals



Name	Function	Type
HOLD	Hold request	Input
HLDA	Hold acknowledge	Output
$\overline{WR}$	Write control	Output, 3-state
$\overline{IO}/M$	IO/memory control	Output, 3-state
$DT/\overline{R}$	Data transmit/receive	Output, 3-state
$\overline{DEN}$	Data enable	Output, 3-state
ALE	Address latch enable	Output
$\overline{INTA}$	Interrupt acknowledge	Output

The 8086 in Minimum Mode

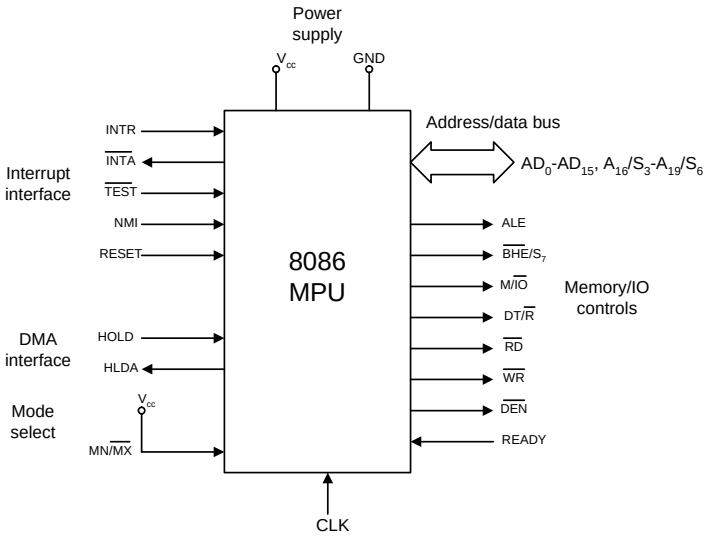
Unique Maximum Mode Signals



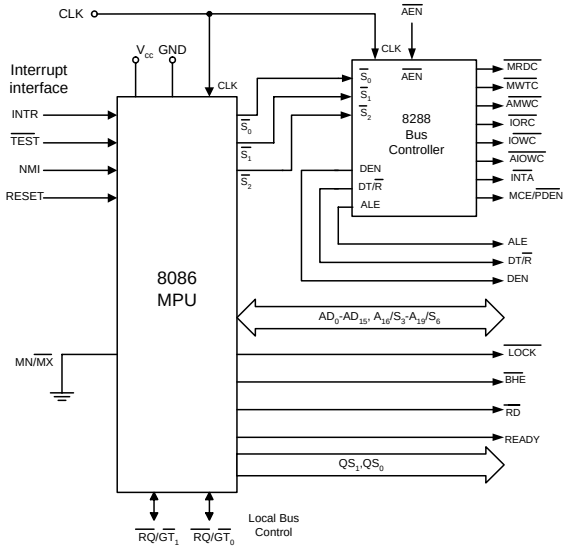
Name	Function	Type
$\overline{RQ}/\overline{GT1,0}$	Request/grant bus access control	Bidirectional
$\overline{LOCK}$	Bus priority lock control	Output, 3-state
$\overline{S2}-\overline{S0}$	Bus cycle status	Output, 3-state
QS1, QS0	Instruction queue status	Output

The 8086 in Maximum Mode

Minimum Mode Interface



Maximum Mode Interface



Microprocessor Buses (I)

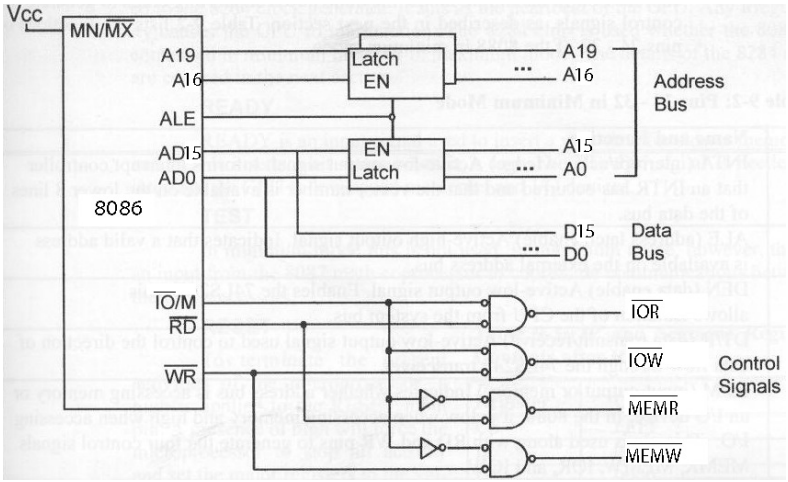
- The 8086 has three sets of separate buses
  - The address bus – provides the path for the address to locate the targeted device.
  - The data bus – transfers data between CPU and the targeted device.
  - The control bus – provides the signals to indicate the type of operation being executed.

Microprocessor Buses (II)

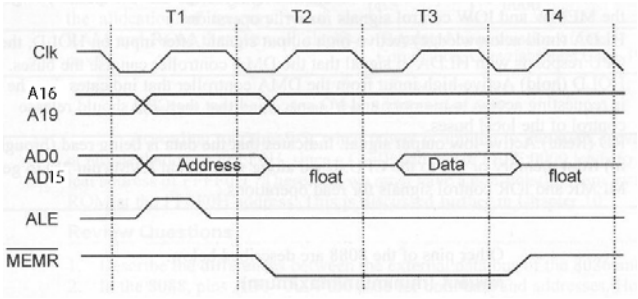
- Address/Data bus
  - The address bus is 20 bits long (A_0-A_{19}).
  - The data bus D_0-D_{15} are multiplexed with address bus A_0-A_{15} -> AD_0 – AD_{15}.
  - The ALE (Address Latch Enable) is set high to indicate the information on AD0-AD15 is address; ALE is low when AD0-AD15 carry data.
  - The process of separating address and data from pins AD0-AD15 is called demultiplexing.
- Control bus
  - There are many controls signals; however, we emphasis on the read and write operations:

$\overline{RD}$	$\overline{WR}$	$\overline{IO}$/M	Signal
0	1	0	$\overline{IOR}$
1	0	0	$\overline{IOW}$
0	1	1	$\overline{MEMR}$
1	0	1	$\overline{MEMW}$
0	0	x	Never happens

Address, Data, and Control Buses in 8086 Based System



Bus Timing of the 8086



The 8086 uses 4 clocks for memory and I/O bus activities.

Read timing:

- The first clock cycle -- ALE latches the address
- The second and third clock cycles – the read signal is provided.
- The end of fourth clock cycle – the data must be at the pins of the CPU to be fetched in.