2102440 Introduction to Microprocessors

Chapter 7

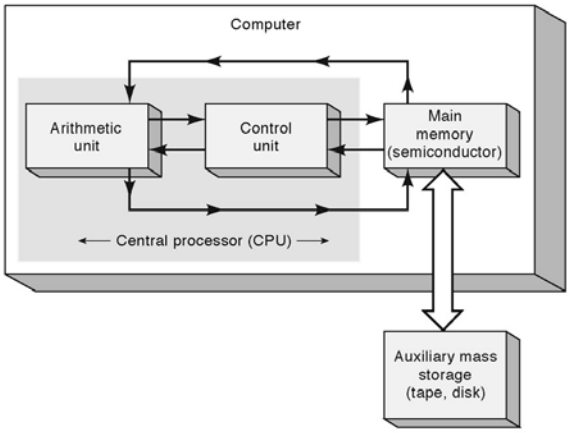
The 8086/8088 Memory and I/O Interfacing

Suree Pumrin, Ph.D.

Topics

- The 8088 and memory
- The 8086 and memory
- The 8086/8088 and I/O

Computer Memory System



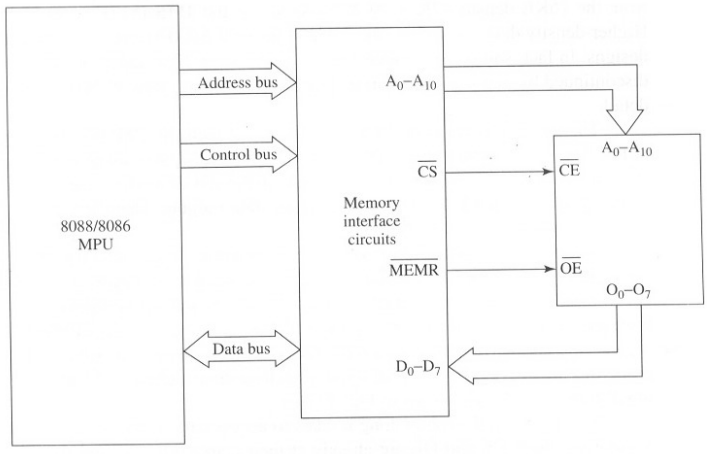
Semiconductor Memory Fundamentals

- Semiconductor memories are used as primary storage for code and data.
- The most widely used semiconductor memories are ROM and RAM.
- Memory capacity
  - Chip capacity -- the number of bits that a semiconductor memory chip can store. While the memory capacity of a computer is in bytes.
- Memory organization
  - The entire chip contains 2^x x y bits – the organization of the memory chip, where x is the number of address pins and y is the number of data pins on the chip.
- Memory speed (access time)
  - The time that data can be accessed from the memory chip.

ROM (Read-Only Memory)

- Nonvolatile memory – contents stay even the power is turned off.
  - PROM (programmable ROM)
  - EPROM (erasable programmable ROM)
  - EEPROM (electrically erasable programmable ROM)
  - Flash memory (Flash ROM)
  - Mask ROM

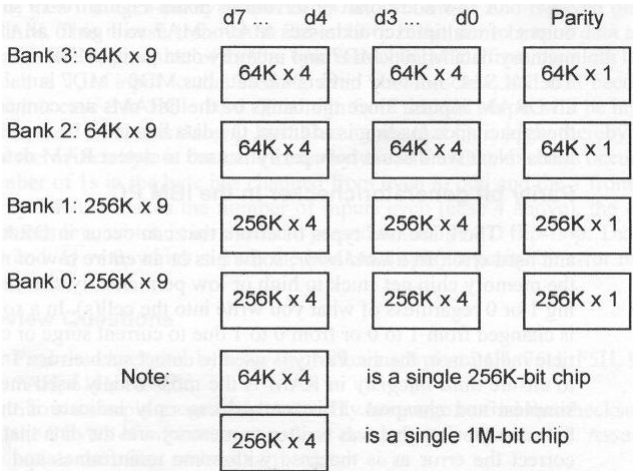
Read-only Memory Interface



RAM (Random Access Memory)

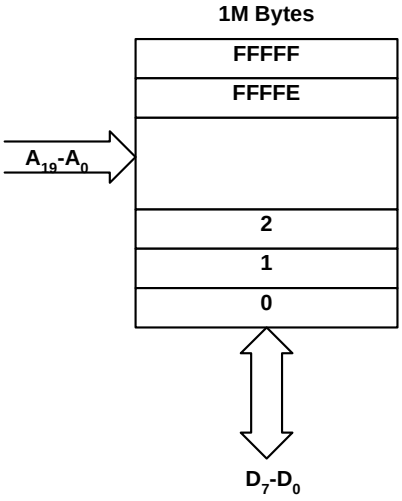
- Volatile memory – data loss when the power's off.
- SRAM (static RAM)
- DRAM (dynamic RAM)
- NV-RAM (nonvolatile RAM)

DRAM Memory Banks



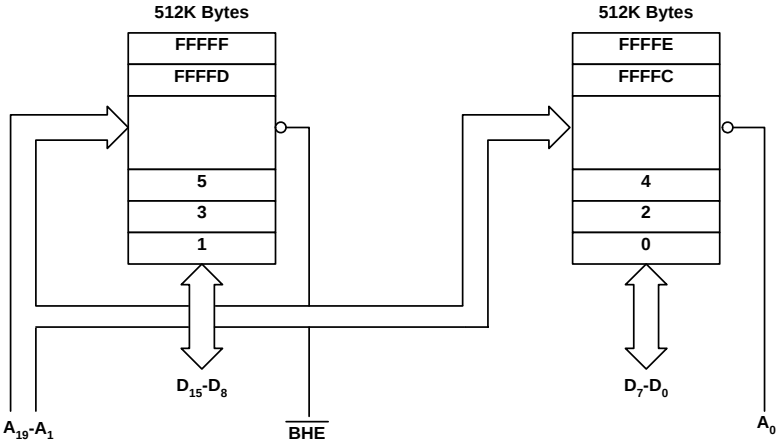
A 640K DRAM

The 8088 Memory Bank



- 1M x 8 memory bank of the 8088
- The byte-wide storage locations are assigned from 00000_{16} – $FFFFF_{16}$
- A 20-bit address is applied to the memory bank over address lines A_0 – A_{19}.
- Bytes of data are transferred between the 8088 and memory over data bus lines D_0 – D_7.

The 8086 Memory bank



There are two independent 512 Kbyte banks: the low (even) bank and the high (odd) bank.

16-Bit Memory Interfacing

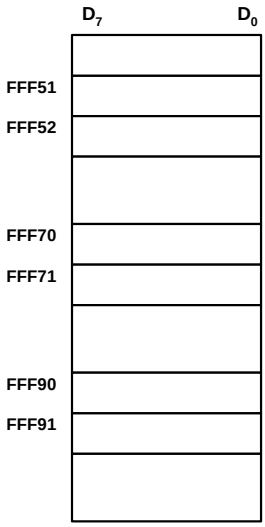
The memory locations 00000-FFFFF are designed as odd and even bytes. To distinguish between odd and even bytes, the CPU provides a signal called $\overline{BHE}$ (bus high enable). $\overline{BHE}$ and A_0 are used to select the odd and even byte, as shown in the table below.

$\overline{BHE}$	A_0		
0	0	Even word	D_0-D_{15}
0	1	Odd byte	D_8-D_{15}
1	0	Even byte	D_0-D_7
1	1	None	

Memory Cycle Time

- Memory cycle time: a bus cycle time used for accessing memory.
  - Memory read cycle time: a time from the CPU provides the addresses at the address pins to the time the data is at the data pins.
  - Wait state: the extra time requested from the CPU to extend the read cycle time when the memory is slow and its access time does not match the memory cycle time.

Accessing Even and Odd words in the 8-bit CPU



Assume that DS = F000

"MOV AL, [FF51]" Odd byte takes 1 MC

"MOV AL, [FF52]" Even byte takes 1 MC

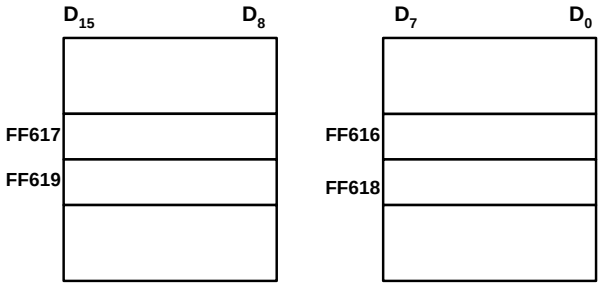
"MOV AX, [FF70]" Even word takes 2 MC

"MOV AX, [FF91]" Odd word takes 2 MC

MC (Memory Cycle)

"Accessing a word is treated like accessing two bytes regardless of whether the address is odd or even."

Accessing a Word in the 16-bit CPU



Assume that DS = F000

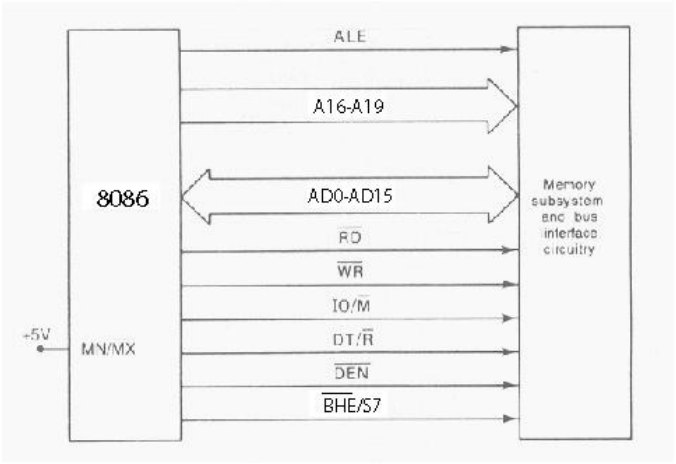
MOV AX, [F617]

1st Memory Cycle (MC)

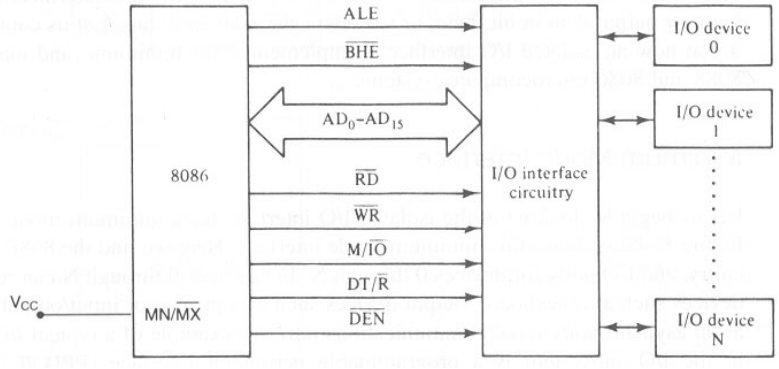
2nd MC

- Accessing a word with an even address takes ONE memory cycle.
- Accessing a word with an odd address requires TWO memory cycles.

Minimum mode Memory Interface



Minimum mode I/O Interface



Byte-wide Output Ports using Isolated I/O