2102440 Introduction to Microprocessors

Chapter 8
Introduction to Other Microprocessors: RISC Processor Architecture

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Topics

- An overview of the architecture of RISC processors for engineers familiar with CISC processors, or engineers new to processor architecture

CISE and RISC

- **CISC**
  - Complex instructions
  - Large instruction set
  - Instructions vary in length
  - Instructions always the same length
  - Instructions execute in a single cycle
  - Focus on doing a lot in one instruction

- **RISC**
  - Simple instructions
  - Small instruction set
  - Instructions always the same length
  - Instructions execute in a single cycle
  - Focus on simple core \( \Rightarrow \) high clock speeds

The MIPS Instruction Sets

- MIPS I
- MIPS II
- MIPS III
- MIPS IV
- MIPS V

32-bit

64-bit

Apple specific
Enhancements

MIPS6

Vendor specific
Enhancements
RISC Processor Block Diagram

Data Flow in RISC Integer Core

Pipelining of Instructions

Problems with Pipelining
Memory Hierarchy: Caching

- CPU Core
- L-Cache
- D-Cache
- Level 2 Cache
- DRAM Main Memory

Associativity of Caches

- Direct Mapped
- 2-Way Set Associative

Memory Mapping

- CPU memory
- Unmapped, Unmapped
- Kernel Mapped, Cached
- Kernel Unmapped, Unmapped
- User Mapped, Cached

Virtual Addresses

- Physical Addresses

Exception Handling

- Exceptions are any interruption to normal operation
  - Interrupts, arithmetic overflow, bus errors, etc
- RISC philosophies apply to exceptions
  - No large tables of vectors
  - MIPS architecture uses two exception vectors
  - Software saves the state and manages nesting
- A software approach gives more flexibility
Accessing Peripherals
- No separate memory and IO space
- Peripherals are memory mapped
- Caching needs to be considered:
  - Uncached access
  - Flush cache before accessing
  - Use special instructions

Optimizing the Performance of RISC Processor Systems
- **Hardware**
  - Keep the pipeline running:
    - Caches
    - Fast memory systems
    - High bus speeds
    - DMA controllers
- **Software**
  - Application-specific
  - DSP enhancements
  - Generic
  - Optimize cache usage
  - Compiler techniques

Summary -- RISC Architectures
- MIPS
- ARM
- PowerPC
- Hitachi SH
- i960