2102440 Introduction to Microprocessors

Lecture 17

80286 Microprocessor

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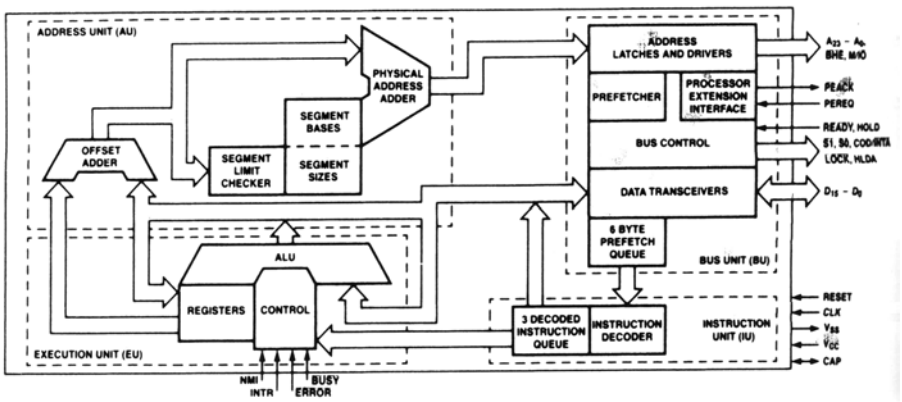
Topics

- Architecture
- 8086 vs 80286 Instruction sets
- Extended instruction sets
- 80286 Interface
- Bus Controller
- Bus Cycle

80286 Microprocessor

- Announced in 1982, the 5th of i86 Family
- 125k transistors, HMOS III technology
- Two mode of operations
  - Real mode – operates as fast 8086/8088
  - Protected mode – enhances memory management, multitasking and protection
- Improves both hardware and software
  - Additional pipeline, demultiplexed address and data bus
  - New enhanced instruction set (upward compat.)
  - Pins are compatible with maximum mode of 8086

Internal Architecture



- 4 independent units (8086 has only two units)
- 24-bit Address bus
- Up to 7 times higher performance than 8086

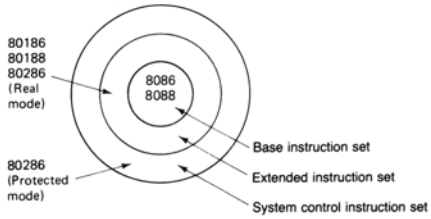
Internal Architecture (Cont.)

- Bus Unit generates all data, address and I/O signals.
  - Prefetcher flushes the prefetched data, if IU finds a branch instruction.
- Address Unit (AU) off-loads address generation, translation and checking from BU.
- Instruction Unit off-loads EU by performing the instruction decoding.
- Execution Unit get the commands form IU, execute the instruction that maybe involve Registers, ALU, AU such as ‘ADD AX, [SI].’

Real Mode Software Model

- All the registers are still there, and MSW (Machine Status Word Register) is introduced.
- The only active bit of MSW in Real Mode is PE (Protected Mode Enable).
- Address space is still the same, 1Mbyte Memory address space (four 64kbyte pages) and 64kbyte I/O space.
- Remember, 80286 has 24-bit address pins physically.

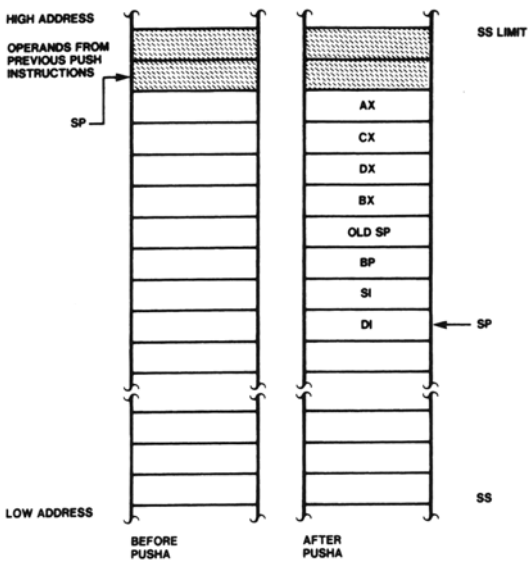
Extended Instruction Set



- 80286 can execute all of 8086 instructions.
- In real mode, 80286 has new instructions plus enhanced old instructions with more addressing mode.
- Only from the 5th member can operate in protected mode.

Format	Operation
PUSH dw/db	Push the specified data word (dw) or sign extended data byte (db) onto the stack.
PUSHA	Push the contents of registers AX, CX, DX, BX, original SP, BP, SI, and DI onto the stack.
POPA	Pop the stack contents into the registers DI, SI, BP, SP, BX, DX, CX, and AX.
IMUL rw, ew, dw/db	Perform the signed multiplication as follows: rw = ew*dw/db where rw is the word size register, ew is the effective word size operand, and the third operand is the immediate data word (dw) or a byte (db).
Instruction db	Perform the logic instruction using the specified byte (db) as the count.
INSB, INSW	Input the byte or the word size element of the string from the port specified by DX to the location ES: [DI].
OUTSB, OUTSW	Output the byte or the word size element of the string from ES: [SI] to port specified by DX.
ENTER dw, 0/1/db	Make stack frame for procedure parameters.
LEAVE	Release the stack space used by the procedure.
BOUND rw, md	Interrupt 5 occurs if the register word (rw) is not greater than or equal to the memory word at md and not less than or equal to the second memory word at md + 1.

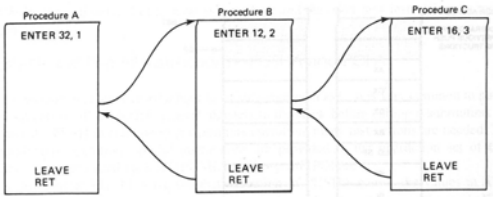
PUSHA / POPA

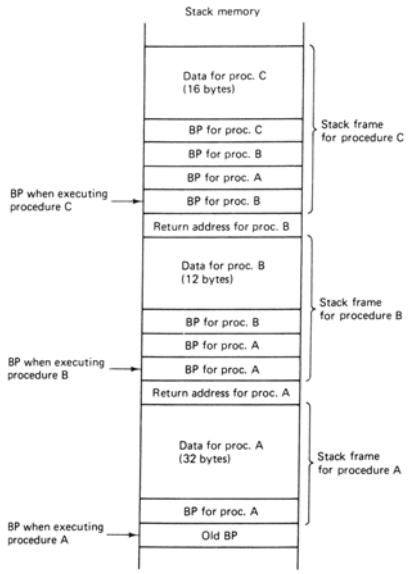


- In high level languages, compilers always push all register to the stack, before calling subroutine.
- New more efficient choice PUSHA, POPA.

Passing Parameters

- Main program may pass parameters of its subroutines through stack – stack frame.
- *'ENTER'* allocates memory in stack for a stack frame, which can be deallocated by '*LEAVE.'*
- Enter has 2 operands, Length of frame, and nesting level.

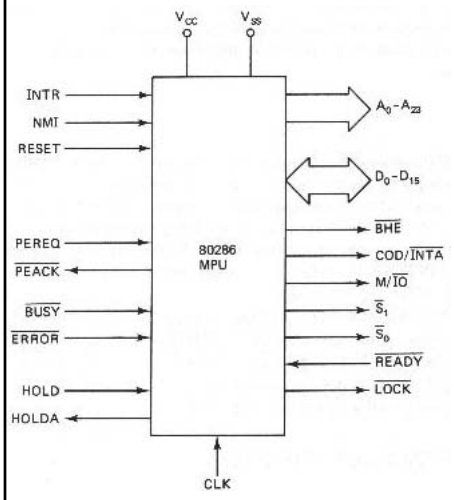




I/O-Memory Transfer

- 8086 can read/write I/O to register AL/AX only, ex. 'IN AX, DX'
- 80286 can read/write I/O to Memory directly, INSB, INSW, OUTSB, OUTSW
- INS?: (ES:DI) ← ((DX))
  (DI) ← (DI) + 1 or –1 (DF=0 or 1)
- REINS?: xxx: INS?
  LOOP xxx

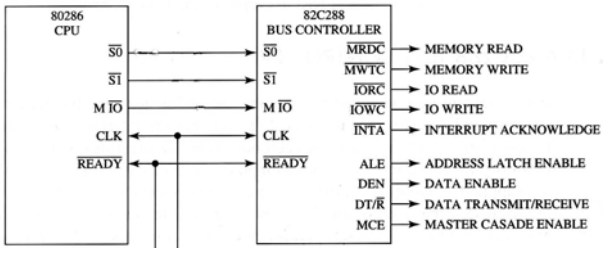
80286 Interface



Mnemonic	Function	Type
CLK	System clock	I
D_{15}-D_0	Data bus	I/O
A_{23}-A_0	Address bus	O
BHE	Bus high enable	O
S_1, S_0	Bus cycle status	O
M/IO	Memory I/O select	O
COD/INTA	Code/interrupt acknowledge	O
LOCK	Bus lock	O
READY	Bus ready	I
HOLD	Bus hold	I
HLDA	Hold acknowledge	O
INTR	Interrupt request	I
NMI	Nonmaskable interrupt request	I
PEREQ	Processor extension request	I
PEACK	Processor extension acknowledge	O
BUSY	Processor extension busy	I
ERROR	Processor extension error	I
RESET	System reset	I
V_{SS}	System ground	I
V_{CC}	System power	I

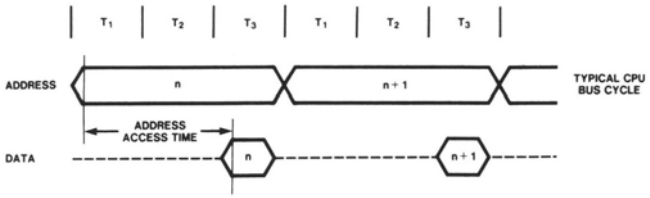
82C288 Bus Controller

As 80286 does provide complete bus control signal, it needs a bus controller.

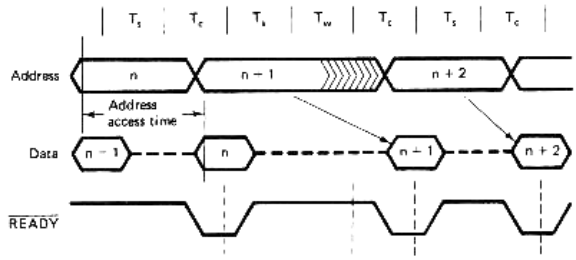


Type of Bus Cycle	M/IO	S1	S0	Command Activated	DT/R State	ALE, DEN Issued?
Interrupt Acknowledge	0	0	0	INTA	LOW	YES
I/O Read	0	0	1	IORC	LOW	YES
I/O Write	0	1	0	IOWC	HIGH	YES
None; Idle	0	1	1	None	HIGH	NO
Halt/Shutdown	1	0	0	None	HIGH	NO
Memory Read	1	0	1	MRDC	LOW	YES
Memory Write	1	1	0	MWTC	HIGH	YES
None; Idle	1	1	1	None	HIGH	NO

Bus Cycle



Conventional Bus Cycle



Pipeline Bus Cycle with wait states

Memory Interface Circuit