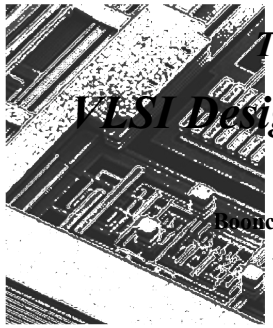


Tutorial 3

VLSI Design Methodology

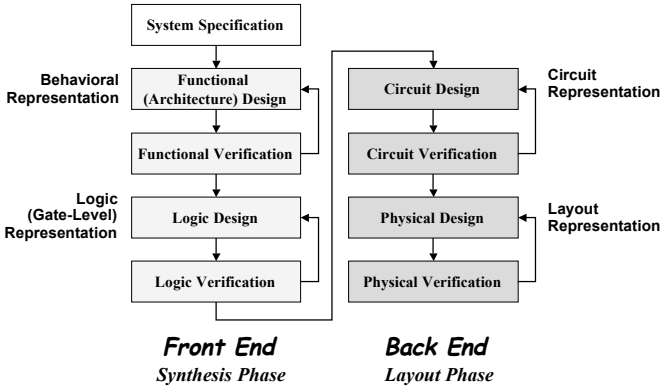
Boonchuay Supmonchai

June 10th, 2006

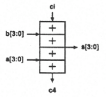
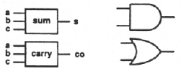
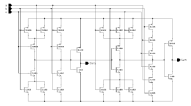
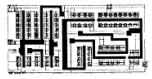
Outlines

- ***VLSI Design Flow and Structural Design Principles***
- VLSI Design Styles
- VLSI Design Strategies
- Computer-Aided Design Technology for VLSI

Simplified VLSI Design Flows



Four Levels of Design Representation

Behavioral Representation		*Functional Blocks, FSM*
Logic (Gate-Level) Representation		*Logic Blocks, Gates*
Circuit (Transistor-Level) Representation		*Transistor Schematics*
Layout Representation		*Physical Devices*

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Structure Design Principles

- ***Hierarchy***:
  - "Divide and conquer" technique involves dividing a module into sub-modules and then repeating this operation on the sub-modules until the complexity of the smaller parts becomes manageable.
- ***Regularity***:
  - The hierarchical decomposition of a large system should result in not only ***simple***, but also ***similar*** blocks, as much as possible.
  - Regularity usually reduces the number of different modules that need to be designed and verified, at all levels of abstraction.

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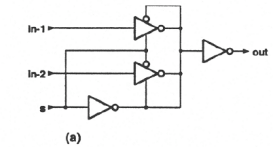
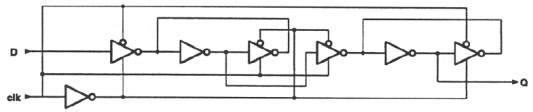
Example of Regularity



2-input MUX

DFF



These circuits are built using inverters and tri-state buffers only.

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Structured Design Principles (Cont.)

- ***Modularity***:
  - The various functional blocks which make up the larger system must have ***well-defined functions*** and ***interfaces***.
  - Modularity allows each block to be designed independently; All blocks can be combined with ease at the end of the process.
- ***Locality***:
  - Internal details remain at the local level.
  - The concept of locality also ensures that connections are mostly between neighboring modules, ***avoiding long-distance connections*** as much as possible.

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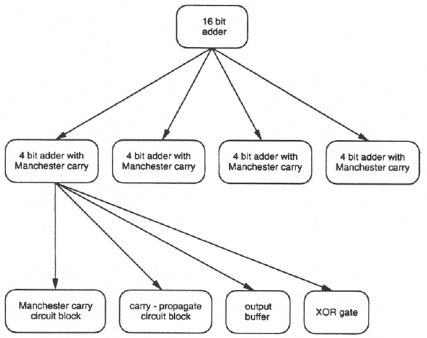
Example: 16-bit Adder Circuit



Structural Hierarchy of a 16-bit Manchester Adder

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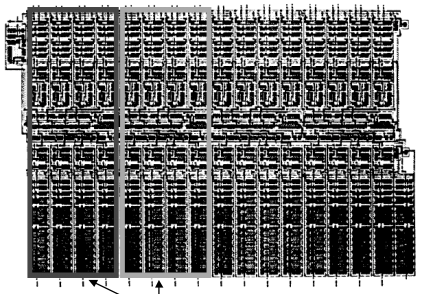
Example (Cont.): Level 1



16-bit Adder Complete Layout

4-bit Adder with Manchester carry

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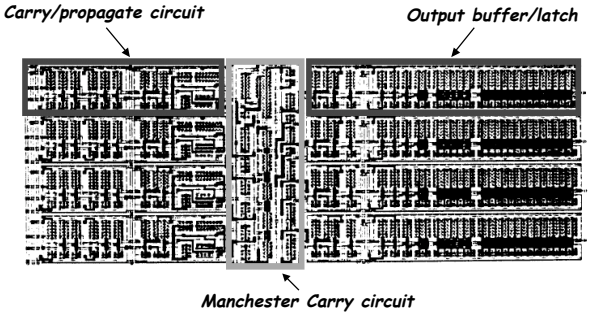
Example (Cont.): Level 2



4-bit Adder with Manchester Carry Layout

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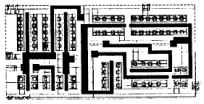
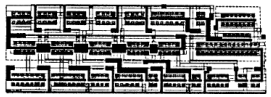
Example (Cont.): Level 3



Carry/propagate circuit layout



Manchester carry circuit layout

Output buffer/latch circuit layout

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Outlines

- VLSI Design Flow and Structural Design Principles
- ***VLSI Design Styles***
- VLSI Design Strategies
- Computer-Aided Design Technology for VLSI

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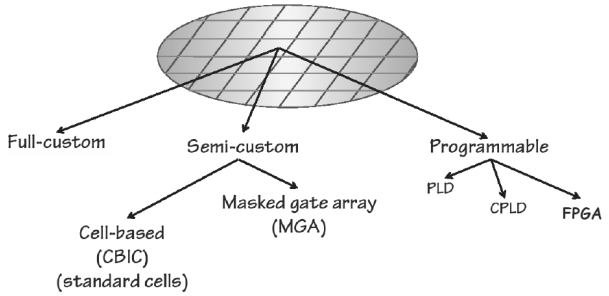
VLSI Design Styles



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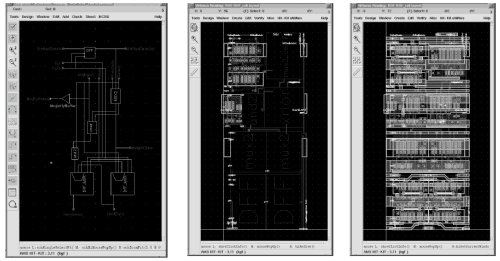
Full-Custom Design

- Full-custom blocks are carefully crafted in the physical level to obtain the highest possible performance.



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Full-Custom Design Key Issues

- The key to Full-custom design is to exploit the fine-grained regularity and modularity in the physical level.
- Manual full-custom design can be very challenging and time consuming, especially if the low level regularity is not well defined.
  - Development cost are too high!
  - Design reuse is becoming popular to reduce design cycle time and development cost. ☞ ***IP blocks***
  - Full-custom design is used only in the critical blocks.

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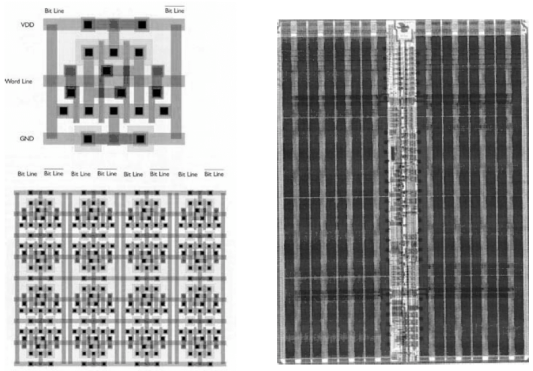
Full-Custom DRAM Example



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Cell-Based Design

- "Lego" Style Design
- All of the commonly used logic cells are developed, characterized, and stored in a standard cell library.
  - Library contains a certain numbers of basic cells such as inverters, NAND, NOR, each in several versions to provide a range of performance.
    - The inverter gate can have standard size, double size, and quadruple size.
- Most popular because of CAD tools availability and capability.

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Cell-Based Design Key Issues

- Inclusion/Exclusion of a gate variation depends on the objectives of the library.
  - Standard Library, Low Power Library, etc.
- Most challenging task is to how to place the individual cells into rows and interconnect them in a way that meet stringent design goals.
  - Most advanced CAD tools have place-and-route tools.
- In a complex, demanding design, standard-cell based design approach may be used as a first pass, then full-custom design where necessary.

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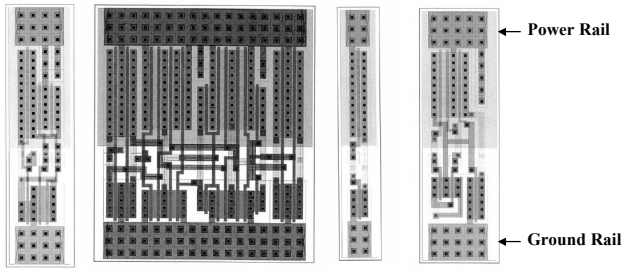
Example of Standard Cells



Each cell layout is designed with a fixed height so that a number of cells can be "snapped" together side-by-side to form rows.

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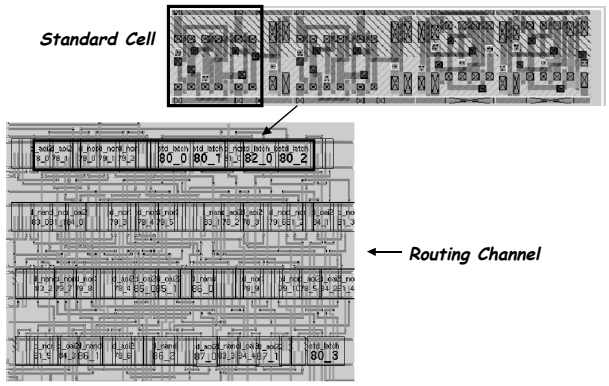
Example of Stand Cells (Cont.)



Cell-Based Design Example

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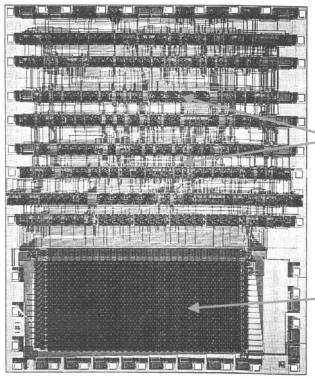

Masked Gate Array (MGA) Design

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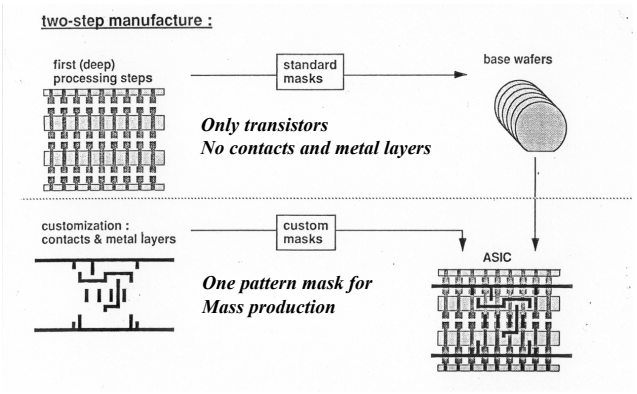

MGA Design Key Issues

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- "Uncommitted" (Unused) transistors or gates are wasted.
  - Performance measured as Chip Utilization Factor ~ used chip area/total chip area.
- Uncommitted cells can be sacrifices to improve intercell routing capability
- Modern GAs use multiple metal layers for channel routing
  - Smaller area, higher density, and routability

Example of MGA Design

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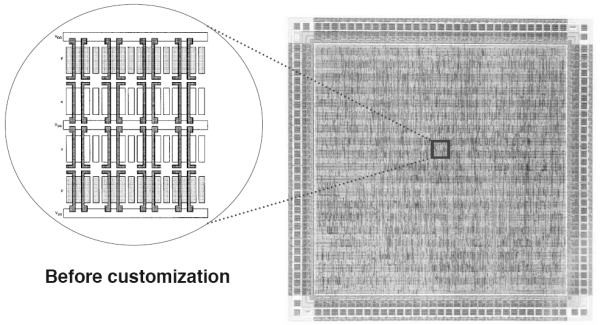

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FPGA Design

- An FPGA chip provides thousands of logic gates, organized into logic blocks, with programmable interconnects.
- To implement a custom hardware, a user can use high-level hardware programming (e.g., HDL).
  - Program logic table for each logic block.
  - Program interconnect switch matrices
  - Program I/O blocks
- Programs last as long as the chip is powered-on

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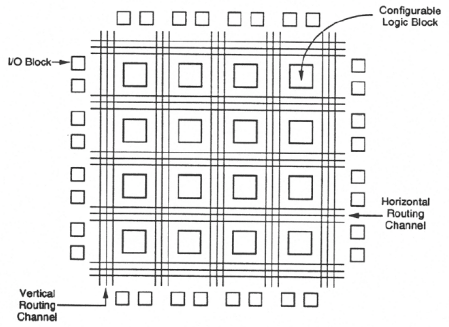
Field Programmable Gate Array (FPGA)



Architecture of Xilinx FPGAs

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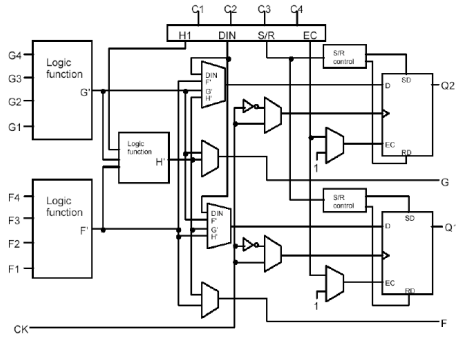
FPGA (Cont.)



Simplified block diagram of a CLB by Xilinx

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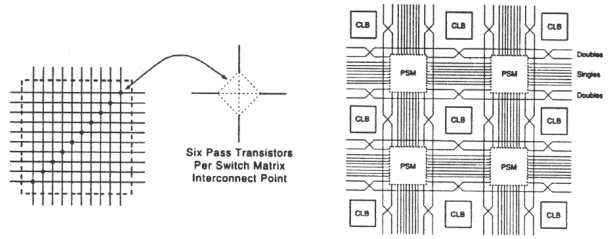
FPGA (Cont.)



Switch matrices and interconnection routing between CLB

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FPGA Design Key Issues

- Chip utilization of an FPGA depends on
  - ***Granularity*** of the logic block - Size of logic block
  - ***Routing capability*** - Size of switch matrices
- The largest advantage of FPGA-based design is the very short ***turn-around time***
  - ***The time required from the start of the design process until a functional chip is available***
- Typical price of FPGA chips is usually higher than other alternatives of the same design, but for small-volume production and for fast prototyping

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HDL-Based Design

1980's

Hardware Description Languages (HDL) were conceived to facilitate the information exchange between design groups.

1990's

The increasing computation power led to the introduction of logic synthesizers that can translate the description in HDL into a synthesized gate-level net-list of the design.

2000's

Modern synthesis algorithms can optimize a digital design and explore different alternatives to identify the design that best meets the requirements.

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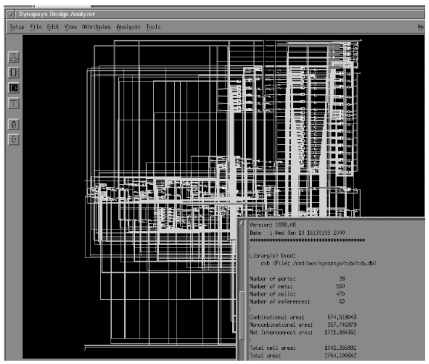
HDL-Based Design Methodology

The design is synthesized and mapped into the target technology.

The logic gates have one-to-one equivalents as standard cells in the target technology.



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Outlines

- VLSI Design Flow and Structural Design Principles
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- ***VLSI Design Strategies***
- Computer-Aided Design Technology for VLSI

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VLSI Design Strategies

- Phenomenal growth rate in VLSI leads to a very complex and lengthy development of ICs.
  - Design complexity increases almost ***exponentially*** with the number of transistors to be integrated.
- Efficient organization of all efforts is essential to the survival of a company.
  - Teamwork
  - Better tools
  - Innovatives and creativities.
  - ***Better Strategies***

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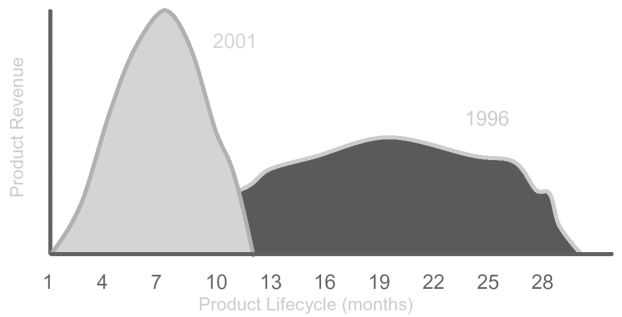
Product Life-Cycle



Products have a shorter life-cycle

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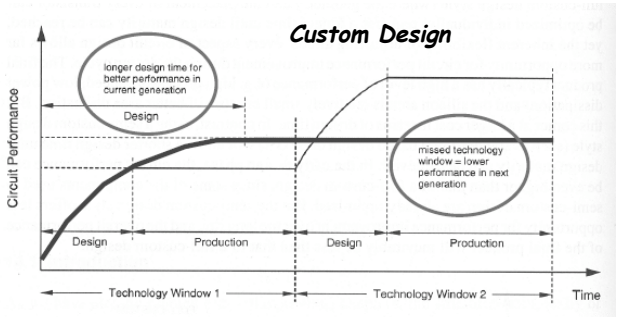
Comparison of Design Strategies

Freedom of Choices….



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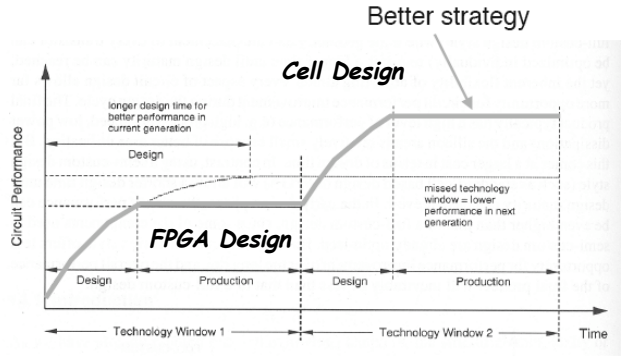
Comparison (Cont.)



System-On-Chip (SOC) Design

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- Integrating all or most of the components of a hybrid system on a single substrate (silicon or MCM), rather than building a conventional printed circuit board.
- Consequences:
  - More compact system realization
    - Less expensive!
  - Higher speed / performance
    - Better reliability

Example of SOC Design

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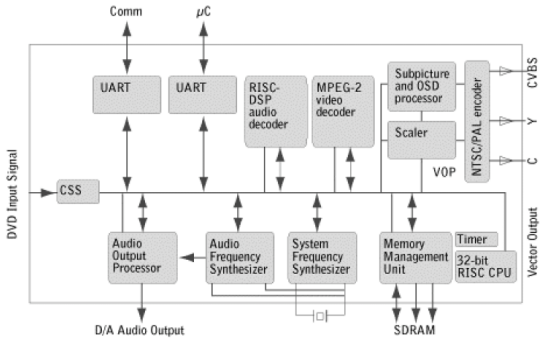

Digital Video Processor

Example of SOC Design (Cont.)

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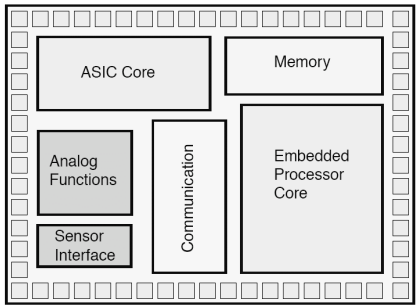

Each functional block can be reused block, IP (Intelectual Property) block, or custom-designed block.

Outlines

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- VLSI Design Flow and Structural Design Principles
- VLSI Design Styles
- VLSI Design Strategies
- ***Computer-Aided Design Technology for VLSI***

Computer-Aided Design Technology

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- CAD tools become more and more indispensable for timely development of ICs.
- Remember! ☞ ***CAD tools are good helpers for time-consuming and computation intensive mechanistic parts of the design, not the creative and inventive parts!***
- CAD technology divides into three categories:
  - ***Synthesis Tools (Synopsys®)***
  - ***Layout Tools (Cadence®)***
  - ***Simulation and Verification Tools***

Synthesis Tools

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- ***High-Level Synthesis*** tools automate the design phase in the top level of the design hierarchy:
  - Based on ***Hardware-Description Languages*** (HDL)
    - **VHDL**, **Verilog**, etc.
  - Determining the types and quantities of modules to be included in the design using accurate estimate of lower level design features (area and delay).
- ***Logic Synthesis and optimization*** tools can then be used to customize the design to particular needs, such as area minimization, low power, etc.

Layout Tools

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- ***Circuit Optimization*** tools deal with the design in the transistor schematic levels:
  - Transistor sizing for delay minimization
  - Reliability issues: process variations, noise.
- ***Layout*** tools concern with the physical level of the design, i.e., how circuits are actually built on the IC:
  - Standard Layout CAD tools are ***Floorplanning***, ***Place-and-route***, and Module generation
  - Sophisticated Layout CAD tools are goal driven and include some degree of optimization functions

Simulation and Verification Tools

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- Time spent on debugging and correcting a design has been increasing ***exponentially*** as each generation passed.
  - Higher penalty is paid if a design flaw is detected later in the design process.
  - Simulation and verification are the most mature area in VLSI CAD
- Goal of all simulation tools is to determine if the design meets the required specifications at a particular design stage.

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Simulation Tools (Cont.)

- Simulation tools used at various stages of the design process are
  - ***Behavior simulation*** tools
  - ***Logic Level simulation*** tools
    - Complement logic synthesis and optimization tools.
  - ***Circuit-level simulation*** tools
    - SPICE or derivatives such as HSPICE, PSPICE, etc.
  - ***Design Rule Checking*** tools
    - Layout rule checking, ***Electrical Rule Checking*** (ERC), reliability rule checking.

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